This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims

1-11 (cancelled)

12. (currently amended) A process of making a data storage device, comprising:

forming a plurality of word lines;

forming a plurality of bit lines; and

forming a first array plane of resistive cross point memory cells, each memory cell coupled to a first respective bit line and coupled to a first respective word line;

forming a second array plane of resistive cross point memory cells, each memory cell coupled to a second respective bit line and a second respective word line, wherein a first memory ~~one~~ cell from the first array plane and a second memory ~~one~~ cell from the second array plane share a common ~~bit line and~~ word line;

biasing the first array so that a current flows between ~~from~~ the common word line and the first respective bit line through the first memory cell from the first array ~~to the common bit line~~;

blocking the current from flowing through the second memory cell from the second array during the biasing of the first array.

13. (currently amended) The process of claim 12 comprising during a ~~the~~ read process forming a unidirectional conductive path between ~~from~~ the common word line and a respective ~~to the~~ bit line through the first memory cell.

14. (currently amended) The process of claim 12, further comprising forming multiple read circuits, each read circuit coupled to one or more of the memory cells by a respective bit line and operable to sense current flow through any memory cell coupled thereto, the current flowing through the common word line.

15. (original) The process of claim 14, wherein each read circuit comprises a sense amplifier.